

Simulation of Software and Heterogeneous Hardware Systems: a Motor Speed Control System Case Study

Breytner Fernández-Mesa, Liliana Andrade, Frédéric Pétrot
 Univ. Grenoble Alpes, CNRS, Grenoble INP*, TIMA, 38000 Grenoble, France
 {breytner.fernandez, liliana.andrade, frederic.petrot}@univ-grenoble-alpes.fr

Index Terms—simulation, architectural exploration, heterogeneous systems, transaction-level modeling, analog and mixed-signal, SystemC

I. DESCRIPTION

Assuring safe interaction among digital, embedded software and physical components in today’s integrated systems is an unavoidable challenge for designers. These systems have applications in the aerospace, automotive, defense, and other industries where small failures could cause great losses — human, economical, etc. Furthermore, their conception, decomposition, implementation, integration and verification has to be achieved within constrained budgets and short time-to-market intervals. To alleviate these issues, domain-specific modeling and simulation tools have emerged and continue to evolve: SystemC [1] is one of such tools.

SystemC and its transaction-level modeling (TLM) and analog and mixed-signal (AMS) extensions [2] allow designers to capture specification in executable models, accelerate development of software with virtual prototypes, explore architectures to accomplish a desired functionality, and validate and verify methods, architecture and integration. Although they have been widely promoted for the development of heterogeneous systems, very few complete case studies are actually available.

To illustrate the architectural exploration capabilities of SystemC and its extensions, we model and simulate an embedded software (digital) and an electrical circuit (analog) version of a DC motor speed control system.

In the digital case, we devise an executable specification and refine it to a virtual prototype composed of a CPU, an instructions memory, an ADC, a DAC and a memory mapped bus (Fig. 1). On this prototype, we develop a control algorithm that is cross-compiled to target a RISC-V ISA [3]. We model the CPU unit with two different technologies: an interpretive model (ISS) and an emulated model (QEMU) [4]; we quantify and compare the effect of both technologies on simulation speed. Simulation results allows us to verify the selected control strategy, parameter values and sampling time, as well as to study the effect of fixed-point and floating point real number representation in the dynamics of the motor speed.

In the analog case, we map the controller equation to timed data flow, signal flow and electric circuit models (Fig. 2), which gives evidence of the suitability of SystemC AMS to

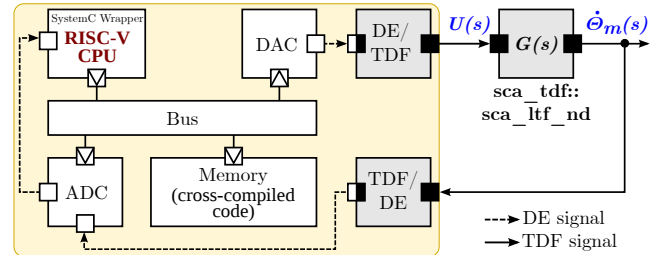


Fig. 1. Digital controller: TLM platform and TDF motor model in close loop.

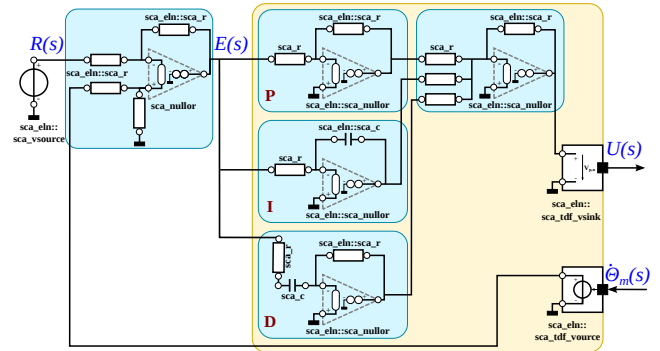


Fig. 2. Analog controller: ELN model of PID.

support a top-down refinement process for analog components. We quantify and compare the simulation speed to an equivalent model built in MATLAB/Simulink.

Our case study illustrates the versatility and performance of SystemC and its extensions in modeling heterogeneous systems, demonstrates coupling of external technologies such as QEMU to speed-up simulation, and exemplifies the early development of code for systems that have not yet been physically implemented. All of these are useful properties that aid system designers take the right software, hardware and analog and mixed-signal choices.

REFERENCES

- [1] IEEE Computer Society, *1666-2011 IEEE Standard SystemC Language Reference Manual*, IEEE, 2012.
- [2] —, *1666.1-2016 - IEEE Standard for Standard SystemC(R) Analog/Mixed-Signal Extensions Language Reference Manual*, IEEE.
- [3] A. Waterman and K. Asanovi, *The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.2*, SiFive Inc. & CS Division, EECS Department, University of California, Berkeley, 2017.
- [4] “RABBITS : an environment for fast and accurate MPSoC simulation.” <http://tima.imag.fr/sls/research-projects/rabbits/>.

*Institute of Engineering Univ. Grenoble Alpes